
RTA-OS ZynqUSA53/ARM

Release Note - Version 5.0.1 (29-10-2018)

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1 Introduction

RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS ZynqUSA53/ARM port plug-in that customizes the RTA-OS development tools for the Xilinx Zynq UltraScale+ Cortex-A53 with the ARM_DS_5_V6 compiler. It supplements the more general information you can find in the *Release Note*.

1.1 Version Information

This is Version 5.0.1 of the RTA-OS ZynqUSA53/ARM plug-in.

1.2 Installation

The installation process is covered in detail in the *ZynqUSA53ARM Port Guide*.

2 **Open EHI Calls**

Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.

3 **Change History**

3.1 **Version 5.0.1**

Additional Features

The following features have been added to this release:

- First Full Release.

Modified Features

The following features have been modified in this release:

- TrustedWithProtection support has been improved to better handle the enabling and disabling of the MPU in interrupts.
- Macros for manipulating the GIC have been moved to the OS.h

Removed Features

No features have been removed from this release.

3.2 **Version 5.0.0 (Preview Release)**

Additional Features

The following features have been added to this release:

- Third Early Access Release.
- Support for Trusted-with-Protection.
- Macros to enable, disable and clear GIC interrupts without corrupting the priority.
- Macros to enable and disable all GIC interrupts on a CPU without corrupting the priority.
- Support for the Autosar ISR source API functions (i.e. ClearPendingInterrupt(), DisableInterruptSource() and EnableInterruptSource()).
- MISRA compliance to conform to the MISRA2012 standard.
- Support for aligning stack to memory protection regions.
- Support for untrusted stack testing at the start of ISRs.
- Target option to detect the Core ID in applications with untrusted code using a GIC register as an alternative to using an SVC call.

Modified Features

The following features have been modified in this release:

- The interrupt vector table labels update to match v1.7 of the UG1085 Zynq UltraScale+ TRM.
- The cross-core interrupts update for the v5.6.x RTA-OS tools.
- The inner ISR wrappers are now core specific.
- Lauterbach Trace32 debug scripts updated for use with Build 92037.
- Core ID detection uses an inline macro rather than a callout function.
- Generic variant now fully tested.

Removed Features

No features have been removed from this release.

3.3 Version 4.99.1 (Preview Release)

Additional Features

The following features have been added to this release:

- Second Early Access release.
- Multi-core support (tested).
- Support for v6.6 ARM DS-5 Compiler.
- CPU interrupt support.
- Spurious interrupt support.
- Non-secure EL0/EL1 support (IPL16).
- Interrupt configuration macros.
- Support function `Os_InitializeGICGroup()` to set GIC interrupt group to 1 for non-secure code.
- Non-secure EL0/EL1 support (IPL16).

Modified Features

The following features have been modified in this release:

- Tests now run on Xilinx UltraScale+ Silicon instead of a simulator.

8 Change History

Removed Features

The following features have been removed from this release:

- Support for v6.4 (and earlier versions) ARM DS-5 Compiler.
- Support for the simulator based variants (ARMA53simulator and GenericRCARx3A53).

3.4 Version 4.99.0 (Preview Release)

Additional Features

The following features have been added to this release:

- Second Early Access release.
- Multi-core support (untested).
- Support for v6.4 ARM DS-5 Compiler.

Modified Features

No features have been modified in this release.

Removed Features

The following features have been removed from this release:

- Support for v6.3 (and earlier versions) ARM DS-5 Compiler.

3.5 Version 1.99.0 (Preview Release)

Additional Features

The following features have been added to this release:

- Initial Early Access release.
- BCC task support, Category 1 and 2 GIC interrupts only (CPU exceptions and spurious interrupt handler not yet supported).
- SC1 Autosar conformance only.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

4 Fixed EHI Calls

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls have been fixed in this release.

5 **Limitations**

5.1 **Installer**

There are the following limitations for the installer:

Limitation	None.
Workaround	None.

5.2 **ZynqUSA53ARM DLL**

There are no known limitations.

6 **Contacting ETAS**

6.1 **Technical Support**

Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see Section 6.2.2).

The best way to get technical support is by email. Any problems or questions about the use of the product should be sent to:

rta.hotline.uk@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- Your .xml, .arxml, .rtaos and/or .stc files
- The command line which caused the error
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The error message you received (if any)
- The file Diagnostic.dmp if it was generated

6.2 **General Enquiries**

6.2.1 **ETAS Global Headquarters**

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6.2.2 **ETAS Local Sales & Support Offices**

Contact details for your local sales office and local technical support team (where available) can be found on the ETAS web site:

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