RTA-OS
Zynq Ultrascale+ R5 with the ARM Compiler

Port Data Sheet

RTA-OS is the ETAS Classic AUTOSAR OS implementation. RTA-OS supports a wide variety of microcontroller/compiler combinations (RTA-OS ports). This port data sheet describes the support for the Cortex-R5 cores of the Zynq Ultrascale+ with the ARM compiler

Supported Devices

RTA-OS supports the Cortex-R5 cores operating in single (lockstep, core 0, core 1) and multicore (core 0 and 1) configurations on the following variants of the Zynq Ultrascale+ microcontrollers:

- XAZU2EG, XAZU3EG, XAZU11EG
- XAZU4EV, XAZU5EV, XAZU7EV
- ZU2CG, ZU3CG, ZU4CG, ZU5CG, ZU6CG, ZU7CG, ZU9CG

Toolchain support

This port supports the following compilers:

- ARM ADS V6.6.2
- ARM ADS V6.6.4 Long Term Maintenance

Interrupt model

On the ZynqUSR5/ARM port, RTA-OS supports up to 32 levels of Category 1 and Category 2 ISRs and user level.

Memory model

On the ZynqUSR5/ARM port, RTA-OS uses the standard flat memory model, following standard EABI.

Memory overhead of RTA-OS

Object	RAM (bytes)	ROM (bytes)
Task	0	20
Cat 2 ISR	0	8
Resource	4	8
Alarm	12	2
Counter	4	20
Schedule Table	16	16
Expiry Point	0	4

Performance

The following gives the key RTA-OS kernel performance data measured in CPU cycles.

Action	Exec time	Ref
Pre-emption	293	A
Normal Termination	162	B
Task Switch	178	C
ChainTask	412	D
WaitEvent	1131	E
SetEvent	1468	F
Schedule	393	G
ReleaseResource	273	H
Cat 2 ISR Entry Latency	252	I
Cat 2 ISR Exit Latency – interrupted task	212	J
Cat 2 ISR Exit Latency – task switch	303	K
Cat 1 ISR Latency	141	L

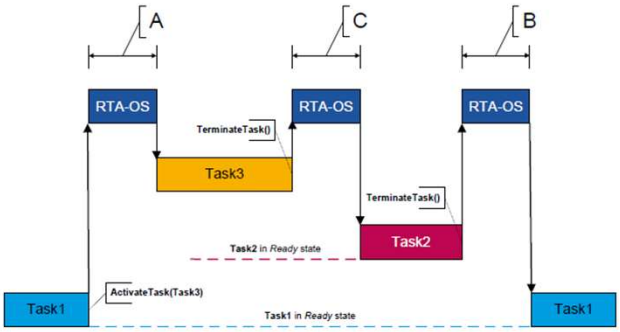

Figure 1 - Task1 is preempted by Task3, followed by a task switch and then normal termination of Task2

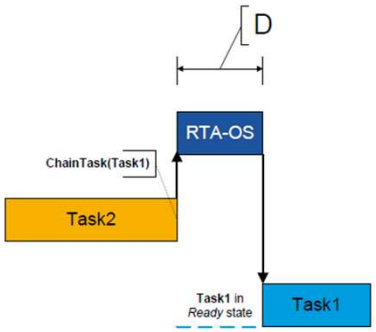

Figure 2 - Task2 chains Task1

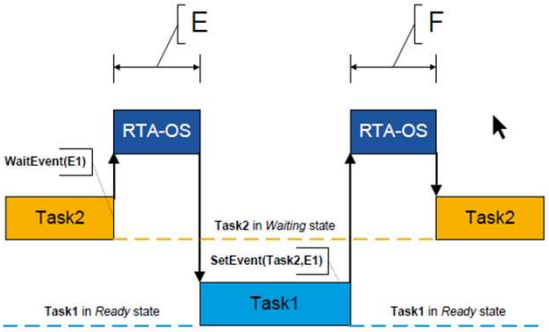

Figure 3 - Task2 waits for an event set by Task1

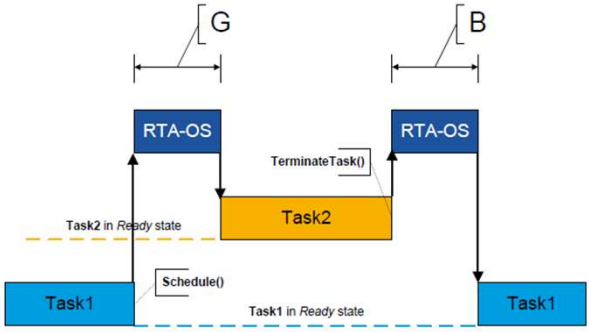

Figure 4 - Task1 allows cooperative scheduling by Task2

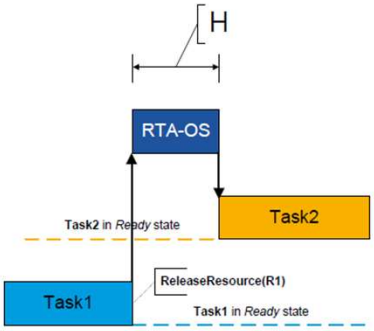

Figure 5 - Task1 releases a resource

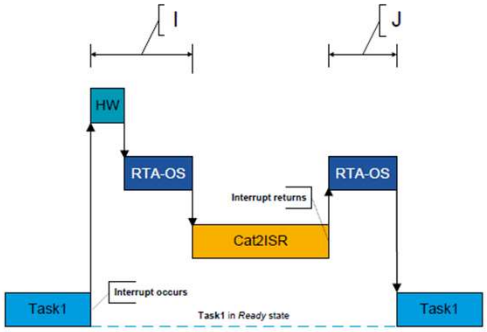

Figure 6 - Category2 ISR entry and exit latency

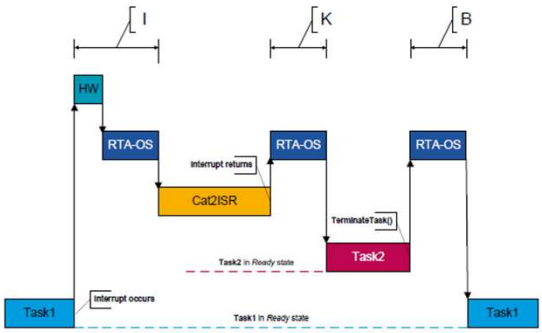

Figure 7 - Category2 ISR switches to Task2

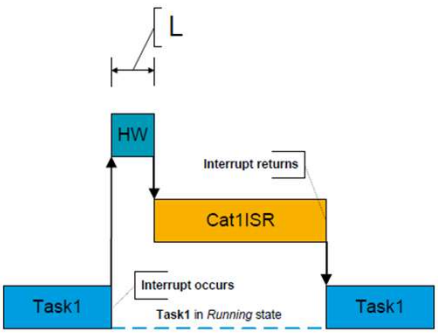

Figure 8 - Category1 ISR entry latency