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Created:	Name Mai	Department MCD/PRM-H	Signature Mir	Date 12.10.2011
Released:	Name Buck	Department EPH1	Signature Bk	Date 13.10.2011

Changes

Revision	Description	Date	Name	Signature
01	222121A010 - initial version	24.10.2006	Mai	Mai
02	222122A010 - Workaround for AUDMBR polling problem [chapter 3.4.1]; Support of ASCET-RP and INTECRIO added [chapter 2.2]	17.07.2007	Mai	Mai
03	222222B010 – Support of new μ C [chapter 2.2]; change of FPGA-Boot-Code due to obsolete components and new lead-free PCB Variant [chapter 3.3.1 & 4.3.1]	30.10.2007	Mai	Mai
04	222222B010 – Support of new μ C [chapter 2.2]	14.11.2008	Mai	Mai
05	22222222B010 – Support of new μ C [chapter 2.2]; introduction of FPGA-B code (H-UDI Interface) [chapter 3.5.2]	13.05.2009	Sz	Sz
06	22222222B010 – Support of new μ C [chapter 2.2]	02.11.2009	Mai	Mai
07	22222222B010 – Support of new μ C [chapter 2.2]	25.05.2011	Mai	Mai
08	23222222B010 - Support of new μ C [chapter 2.2] - change of EPLD Code [chapter 3.2]	12.10.2011	Mai	Mai

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1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the required tool-chain to use this ETK.

Two different items are described.

- Explanation of the version-system of the ETKS6.0
- The required versions of software (INCA / ASCET) , HSP (calibration hardware firmware of e.g. ES59x, ES690, ES1232, ...) and ETK - hardware.

Additionally other requirements for running the ETK.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK

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2 Tool-Chain Information

2.1 Version-Syntax of the ETKS6.0

The ETKS6.0 version information is located on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The old version information has the following syntax: **aabb cc₁deee/ff**

The new version information has the following syntax: **aabb cc₁cc₂deee/ff**

PLD-Code Information:

aa: EPLD-Code version (10, 11, 12...)	see chapter 3
bb: FPGA-Boot-Code version (10, 11, 12...)	see chapter 3
cc₁: FPGA-A-Code version (10, 11, 12...)	see chapter 3
cc₂: FPGA-B-Code version (10, 11, 12...)	see chapter 3

Hardware-Information:

d : PCB version (A, B, C, ...)	
eee: Hardware state of the PCB (010, 011, 012, ...)	see chapter 4
ff: Assembly variant of the PCB (00, 01, 02, ...)	

The first delivered hardware state of the ETKS6.0 was **222121A010/00**.

2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.

If you have any problems to get this ETK running please contact our local customer support or sales representative.

Hardware:

Name	Needed version	Remarks
ES690	V 10.1.0	Supported
ES59x	V 10.1.0	Supported
ES910.2	HSP V5.1.1	Supported
ES1000.2/3 – system	V 10.1.0	Supported with ES1232
MAC2, ES1000.1, ES1200/01, and ES1231		Not supported

Software:

List of supported Renesas microcontroller:

Microcontroller	HSP	INCA	ETK Drivers and Tools	ASCET-RP	INTECRIO
SH72512 ¹⁾	V5.1	V6.1.0	n. a.	V5.6.0	V2.1
SH72512FCC ¹⁾	V5.1	V6.1.0	n. a.	V5.6.0	V2.1
SH72513 ¹⁾	V5.1	V6.1.0	n. a.	V5.6.0	V2.1
SH72513FCC ¹⁾	V5.1	V6.1.0	n. a.	V5.6.0	V2.1
SH72531F ²⁾	V7.1.3	V6.2.1	V2.1.2	V6.0.1	V3.1
SH72531FCC ²⁾	V7.1.3	V6.2.1	V2.1.2	V6.0.1	V3.1
SH72531RFCC ¹⁾	V7.1.3	V6.2.1	V2.1.2	V6.0.1	V3.1
SH72533FCC ²⁾	V7.1.3	V6.2.1	V2.1.11	V6.0.1	V3.1
SH72543R ¹⁾	V7.1.3	V6.2.1	V2.1.3	V6.0.1	V3.1
SH72544 ¹⁾	V5.1	V6.1.0	n. a.	V5.6.0	V2.1
SH72544R ¹⁾	V7.1	V6.2.1	V2.1.0	V6.0.1	V3.1
SH72546RFCC ¹⁾	V5.1	V6.1.0	V1.1.1	V5.6.0	V2.1
SH72567BFCC ¹⁾	V7.1.3	V6.2.1	V2.1.13	V6.0.1	V3.1
SH72569BFCC ¹⁾	V7.1.3	V6.2.1	V2.1.13	V6.0.1	V3.1

¹⁾ Configuration A (FPGA-A-Code) : Interface AUD

²⁾ Configuration B (FPGA-B-Code) : Interface H-UDI

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3 PLD-Code Changes

3.1 General remarks to this chapter

The programmable logic code within the ETKS6.0 is stored onto programmable logic devices (FPGA and EPLD). For the version syntax please refer to chapter 2.1.

3.2 EPLD-Code version 2.2 was the first delivered version

3.2.1 Details of change

Version 2.3: file dated 12.01.2010
Changes: Initialization problem during manufacturing test fixed

3.2.2 Delivery condition

The EPLD version **2.3** will be programmed into all shipments.

3.3 FPGA-Boot-Code version 2.1 was the first delivered version

3.3.1 Details of change

Version 2.2: file dated 04.07.2007
Changes: Due to a PCB change to a lead-free Version with the replacement of obsolete components, the Boot Code has to be adapted in order to support new components.

3.3.2 Delivery condition

The FPGA-Boot version **2.2** will be programmed into all new shipments.

3.4 FPGA-A-Code version 2.1 was the first delivered version

3.4.1 Details of change

Version 2.2: file dated 04.07.2007
Bug fixes: Includes workaround which avoids failure of AUD-II interface occurring if polling is retried immediately after the timeout. Without this workaround programming the ECU Flash via ETK could fail. Missing samples or unexpected extra samples could occur during measurement.
Remedy: New FPGA code fixes the problem.

3.4.2 Delivery condition

The FPGA A version **2.2** will be programmed into all new shipments.

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3.5 FPGA-B-Code version 2.2 was the first delivered version

3.5.1 No change

Version 2.2: file dated 07.05.2009

3.5.2 Delivery condition

The FPGA B version **2.2** will be programmed into all new shipments.

Note: FPGA-B-Code has to be switched from the default delivery condition!

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4 Hardware Changes

4.1 General remarks to this chapter

Hardware problems or obsolete parts can make it necessary to change the manufacturing of this ETK. Information about the changes is listed underneath. The hardware-state starts with version A010. For the version syntax please refer to chapter 2.1.

4.2 Changes from Hardware-state A010 to version B010

4.2.1 Details of Change

Changes: HW had to be redesigned due to obsolete components. The electrical characteristics remained the same!
This new Hardware is RoHS-compliant.

4.2.2 Delivery condition

The hardware-state **B010** will be delivered with all new shipments.
A-Revision ETKS6.0 can not be upgraded to the B-Revision!

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5 Abbreviations

ETK	Emulator test probe
ES1000	VME - system, successor of INCA-VME
INCA-VME	Old VME - system for MC and RP
ES690	MC hardware, successor of MAC2
MAC2	Old MC hardware
INCA	MC software, successor of VS100
VS100	MC software
ETK Configuration Tool	Configuration Software, in order to configure an ETK, successor of the old DOS tool
DOS ETK-Config-Tool	Old configuration software, in order to configure an ETK
HSP	H ardware S ervice P ack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
Firmware	Software for MC hardware; necessary for implementation of new features or bugfixes
Hotfix	Software bugfix for a refresh version
Tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	M easurement & C alibration
RP	R apid P rototyping
PLD	P rogrammable L ogic D evice
FPGA	F ree P rogrammable G ate A rray; interface component to the application hardware
PCB	P rinted C ircuit B oard
DPR	Dual Ported RAM; special RAM onto the ETK which allows an access from ECU and application hardware at the same time
/CS	Chip select