Product :	BR_XETK-S2.0A			
Title :	Release Notes			
File :	BR_XETK-S2.0A_Release-Notes.docx			
TTNR :	F-00K-109-477			
Comments :	Current shipped hardware state: **A013/01** Current released firmware version: **HSP 11.13.0**			
Created:	Name M. Higgins	Department NE/EHE3	Signature M. Higgins	Date 2019-06-25
Released:	Name T. Collins	Department NE/EHE3	Signature T. Collins	Date 2019-06-25

Changes

Revision	Description	Date	Name	Signature
01	Initial Version	2015-02-11	Mai	Mai
02	Updated CPLD/HDC/Firmware with HSP 10.9	2015-06-14	M. Higgins	M. Higgins
03	Updated HDC/Firmware with HSP10.10; new units manufactured with hardware state A013.	2015-09-29	M. Higgins	M. Higgins
04	Updated HDC/Firmware with HSP 10.11	2015-12-18	M. Higgins	M. Higgins
05	Updated HDC/Firmware with HSP 11.0.0	2016-03-29	M. Higgins/ T. Collins	M. Higgins/ T. Collins
06	Updated Firmware with HSP 11.1.0	2016-06-28	M. Higgins	M. Higgins
07	Updated Firmware with HSP 11.2.0	2016-09-27	M. Higgins	M. Higgins
08	Updated microcontroller support table	2017-03-28	M. Higgins	M. Higgins
09	Updated Firmware with HSP 11.8.0	2018-03-20	M. Higgins	M. Higgins
10	Updated Firmware with HSP 11.13.0, updated microcontroller support	2019-06-25	M. Higgins	M. Higgins

Table of content

1 General Information

1.1 Safety Notice

Calibration activities influence the behavior of the ECU and the systems controlled by the ECU. This may result in unexpected behavior of the vehicle and thus can lead to safety critical situations. Only well trained personnel should be allowed to perform calibration activities.

1.2 System Requirements

Recommended system requirements on a PC running ETK Drivers and Tools, HSP or Inca:

- 2 GHz Pentium-PC or equivalent, equipped with
  - 1 GB RAM (basic hardware), depending on the use cases 2GB RAM are advantageous
  - Hard disk with minimum 10 GB free disk space
  - DVD-ROM for installation
  - XGA-Graphic card with XGA-screen and resolution of at least 1024 x 768 with 16 bit colors, DirectX 7
  - Fast Ethernet adapter 100BaseT
    - with full duplex capability
    - configured as component TCP/IP only
    - separate to e.g. company network
  - WINDOWS® XP (SP3 or higher), WINDOWS®VISTA (SP1 or higher) or WINDOWS®7

1.3 Restrictions

WINDOWS® 95b, WINDOWS® NT, WINDOWS® 2000 and WINDOWS® 98SE are not supported.

1.4 Miscellaneous

To ensure the highest data throughput from the XETK device up to the PC system no other PC software should be run via this Ethernet adapter.

2 Version Syntax and Tool-Chain Information

2.1 Version-Syntax of the BR_XETK-S2.0A

The BR_XETK-S2.0A hardware version information is located on the product sticker and can be read out of the XETK using the firmware update tool HSP or XETK Configuration Tool.

Hardware State Syntax: **abbb/cc**

Description (modification details refer chapter 5)

a	PCB Version (A=V1.0, B=V1.1, C=V1.2, ...)
bbb	PCB Hardware State (010, 011, 012, ...)
cc	PCB Population Variant (00, 01, 02, ...)

The BR_XETK-S2.0A Firmware version information can be read out of the XETK using the firmware update tool HSP or XETK Configuration Tool. It is not printed onto a XETK sticker.

Firmware-Version Syntax: **aaa.bbb.ccccc**

Description (modification details refer chapter 5)

aaa	Major Release (0...255)
bbb	Minor Release (0...255)
ccccc	Revision/Patch (0...65535)

Firmware Packages:

HDC Work	aaa.bbb.ccccc
Firmware Work	aaa.bbb.ccccc
HDC Rescue	aaa.bbb.ccccc
Firmware Rescue	aaa.bbb.ccccc
CPLD	aaa.bbb.ccccc

2.2 Version information of the tool-chain components

To use this XETK with the other components of the tool-chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.
If you have any problems putting the XETK into operation please contact our local customer support or sales representative.

Updates or refreshes can be downloaded from the ETAS homepage:
http://de.etasgroup.com
http://en.etasgroup.com

2.3 Software and microcontroller support

Microcontroller	HSP	INCA	ETK Tools	ASCET-RP	INTECRIO
MPC5744K(-ED), SPC/EMU574K72	V10.7.0	V7.1 SP7	V4.0.3	V6.3	V4.5
MPC5746M(-ED), SPC/EMU57EM80	V10.7.0	V7.1 SP7	V4.0.3	V6.3	V4.5
MPC5777A(-ED), SPC/EMU57HM90xy	V10.7.0	V7.1 SP7	V4.0.3	V6.3	V4.5
MPC5746R(-ED)	V10.7.0	V7.1 SP7	V4.0.3	V6.3	V4.5
SPC/EMU58NE84	V10.9.0	V7.1 SP9	V4.0.5	V6.3	V4.5
SPC/EMU58NN84	V11.2.0	V7.2 SP2	V4.1.3	V6.3	V4.5
SPC58xG	V11.13.0	V7.2 SP13	V4.1.14	V6.3	V4.5

MPC5xxx: Freescale microcontroller device
SPC/EMU5xxx: STMicroelectronics microcontroller device

3 What's New - Release Notes

This chapter lists the main improvements compared to a previous shipped ETK product. Additionally a detailed list of already known issues can be found here.

3.1 New or Enhanced Functions

3.1.1 In HSP 11.13.0

Feature	Description
Correction of TFS# 611323	XETK updated to only write the Distab17 Event List when measurement is started.

3.1.2 In INCA 7.2.13, ETK Tools 4.1.14

Feature	Description
Additional microcontroller support, Jira: ETKPRG-328	Initial support of cpu type: SPC58xG

3.1.3 In ETK Tools 4.1.9, HSP 11.8.0

Feature	Description
LertV3, TFS #582556	Added support for LERTv3. (reconfigurable size emulation memory)

3.1.4 In INCA 7.2.2, ETK Tools 4.1.3

Feature	Description
Additional microcontroller support	Initial support of cpu type: SPC/EMU58NN84

3.1.5 In HSP 11.2.0

Feature	Description
XCP Debugging Enhancement	Increased JTAG clock when playing debug sequences.
Correction of TFS# 538954	Bypass counter is now incremented based on the value already set in ECU, not starting from 0.
Correction of TFS# 513584	Distab17 change counter and event header now updated properly when Distab17 is used together with timer triggered rasters.
Correction of TFS# 534959	Update to ensure INCA measurement does not stop if an RP system accesses an XETK event configured for both DAQ and STIM.

3.1.6 In HSP 11.1.0

Feature	Description
XCP Debugging Enhancement	New User Command: DBG_SEQUENCE_MULTIPLE
Correction of TFS# 517066	Update of OMD handling to ensure XETK allocates only available calibration handles
Correction of TFS# 495909	Performance improvements for DISTAB 17 initialization for coldstart measurements.
Correction of TFS# 515424	Update to support MCE measurements in case of ECU being power cycled during running MCE measurements.

3.1.7 In HSP 11.0.0

Feature	Description
Correction of TFS# 462578	Update of OMD handling to cover use cases where the OMD has been cleared by ECU software, without a standby power failure.
Correction of TFS# 509978, 509968, 510314	Update to XETK heap memory handling to avoid sporadic communication issues such as: • Freezing working data causes connection interrupt • SET_DAQ_PTR error when changing experiments • After reconfiguration, measurement is not possible for DISTAB17
Correction of TFS# 513135	Update of DISTAB17 event list handling for 3rd party use case. Event list entries will be written when DAQ lists are started, also after subsequent resets while DAQ is running.
Correction of TFS# 510041	Update to ensure measurement restarts correctly after ECU power interruption.
Correction of TFS# 516992	Correction to the calculation/display of the BR_XETK firmware monitor variable: CRC error counter.
Correction of TFS# 520136	Update of OMD handling whereby the OMD check fails if OMD on ECU is corrupt or initialized with certain values

3.1.8 In HSP 10.11

Feature	Description
Correction of TFS# 470875	Update to reduce timestamp jitter in high priority rasters during heavily loaded measurement experiments. The issue had occurred only under specific conditions.
Correction of TFS# 433552	Update to Nexus/JTAG module byte counter, to make more efficient ECU access.

Correction of TFS# 493482	Update to ensure proper timestamps in measure file after using INCA file recovery mechanism.
Watchdog Control Enhancement (TFS# 483151)	Interface extended to support additional watchdog pin control command.
Service Based Bypass (TFS# 484227)	Initial support for Service Based Bypass V2.1. Requires Intecrio V4.6 or higher. Requires ASCET-RP 6.4 or higher.

3.1.9 In HSP 10.10

Feature	Description
Correction of TFS# 474328	Ensure handshake bits (Data valid and RAM valid) are updated properly under all conditions. With HSP 10.8.x and HSP 10.9.x the bits may reflect the wrong state when the XETK standby supply supervision feature is configured to “No Standby Supply”.
Correction of TFS# 468020	This is the final solution for TFS# 459543 listed below, in the HSP 10.8.1 section. Event based rasters occurring with a slower rate than described the a2l file will have the same update rate as was available with HSP 10.8 or older.

3.1.10 In HSP 10.9

Feature	Description
Correction of TFS# 454880	Ensure XETK failsafe HSP update of FW & HDC works under all conditions.
Correction of TFS# 438441	Enhanced debug sequence timing for 3rd Party Debug API.
Correction of TFS# 451988	Only turn off Green LED / allow page switch after all statically configured overlay handles are initialized with RP values.
Configuration of JTAG access path	Additional configuration feature “ETKAS1ToUCAS”, for selecting the primary core used on JTAG accesses. As with (F)ETK, the feature is not displayed in the XETK Configuration Tool and can only be set via A2l file. The following values are possible, but not necessarily valid on all cpu types: “ETKAS1ToUCAS” “0x2A” -> Core 2 “ETKAS1ToUCAS” “0x29” -> Core 1 “ETKAS1ToUCAS” “0x28” -> Core 0 The default value of the XETK is Core 2, suitable for all cpu types except “MPC5746RED”. To continue using the cpu type “MPC5746RED”, the A2l file must

	be updated and the combination HSP10.9 / INCA 7.1.9 must be used. The A2l file and ProF configuration must contain the following key / value configuration pair: “ETKAS1ToUCAS” “0x29”. The feature is introduced to support specific use cases, i.e. MPC5746R single core. For this use case the A2l file must contain the following key / value configuration pair: “ETKAS1ToUCAS” “0x28”. This configures the XETK to use Core 0 as the primary path for measurement/calibration. The configured core must be accessible when the ECU/XETK handshake is finished.
Configuration of /TRST behavior	Additional option for feature “JTAG /TRST Control”, necessary for hitting debugger breakpoints on internal software resets. Debugger must be configured to only monitor /RESETin and XETK configured for “2”, which is XCT option “Asserted with /RESETin”.
Correction of TFS# 459543	Updated to ensure measurement continues as expected. With this FW, event based rasters occurring with a slower rate than described the a2l file may have a choppy visual update in the INCA EE. Recorded data will have the proper timestamp.
Correction of TFS# 440609	While configured for fixed/static emulation and without running INCA, the XETK had been inadvertently copying the RP to the WP on start-up. With the correction, the RP is only copied to the WP when a power failure occurs.
Correction of TFS# 419281	Increased polling rate of JIN/JOUT register in order to improve handshake timing

3.1.11 In INCA 7.1.9

Feature	Description
Correction of TFS# 460183	Check sum has an erroneous result when MEMORY_SEGMENT is overlapping address 0x09000000.
Additional microcontroller support	Initial support of cpu type: EMU58NE84_Rev1

3.2 Known issues

Please contact ETAS for further information about known issues listed below.

3.2.1 In HSP 10.9.x and HSP 10.10.0

Issue Identifier	Description
TFS# 470875	In specific measurement configurations, there may be an increase in the timestamp jitter. No

	measurement data is lost. Solution planned for HSP 11.0.

3.2.2 In HSP 10.8.0 and older

Issue Identifier	Description
TFS# 454880	XETK is unable to boot in rescue mode under certain conditions.

4 Product Variants

The BR_XETK-S2.0A can be purchased in one variant. For details refer to the user guide.

5 Hardware Modifications

5.1 General remarks to this chapter

Hardware issues or obsolete parts can make it necessary to modify the population of the XETK. The first released version, available modifications, and current version are listed below. For the version syntax please refer to chapter 2.1.

5.2 First delivered version

The hardware state **A012/01** is the first delivered version.

5.3 Current delivery condition

The hardware state **A013/01** will be delivered with all new shipments.

This version includes an updated XETK system RAM. There is no functional difference for the user as compared to the prior delivered version. An update from A012/01 to A013/01 is not necessary.

6 Firmware Modifications

6.1 General remarks to this chapter

The programmable logic code within the BR_XETK-S2.0A is stored onto programmable logic devices (FPGA, Firmware, and CPLD). The first released version and current version are listed below. For the version syntax please refer to chapter 2.1.

6.2 First delivered version

FPGA Work	1.0.5511
Firmware Work	1.0.19
FPGA Rescue	1.0.5511
Firmware Rescue	1.0.19
CPLD	1.0.1

6.3 Current delivery condition

The following firmware versions will be programmed into all BR_XETK-S2.0A shipments:

FPGA Work	1.0.20
Firmware Work	1.0.48
FPGA Rescue	1.0.20
Firmware Rescue	1.0.48
CPLD	1.0.3

In case of any problems the above mentioned firmware can be programmed to the XETK by using HSP 11.13.0. This HSP version is similar to the currently delivered XETK products. Newer HSP versions could contain bug fixes and / or new features.

Attention: For updating the XETK - FPGA with a later version by using the HSP Firmware update tool, all XETK - packages will be updated one after another and will last a few minutes.

7 Abbreviations

XETK	Product (emulator test probe) which can directly be connected to the tools PC
INCA	Measurement and Calibration Software of ETAS
ASCET-RP	Rapid Prototyping Software of ETAS
INTECRIO	Rapid Prototyping Software of ETAS
XETK Configuration Tool	Configuration Software, in order to configure a XETK
HSP	**H**ardware **S**ervice **P**ack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
firmware	Software for MC hardware; necessary for implementation of new features or bug fixes
Hot-fix	Software bug-fix for a refresh version
tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	**M**easurement & **C**alibration
RP	**R**apid **P**rototyping
CPLD	**C**omplex **P**rogrammable **L**ogic **D**evice
FPGA	**F**ield **P**rogrammable **G**ate **A**rray; interface component to the application hardware
PCB	**P**rinted **C**ircuit **B**oard
DPR	Dual Ported RAM; special RAM onto the ETK which allows an access from ECU and application hardware at the same time
/CS	Chip select