

# ES4350.1 Carrier Board

## User's Guide

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# Contents

|              |                              |    |
|--------------|------------------------------|----|
| <b>1</b>     | ES4350.1 Carrier Board       | 5  |
| <b>1.1</b>   | Features                     | 5  |
| <b>1.2</b>   | Block Diagram                | 7  |
| <b>1.3</b>   | Hardware Features            | 8  |
| <b>1.3.1</b> | Carrier Board for Piggybacks | 8  |
| <b>1.3.2</b> | Synchronization Signals      | 8  |
| <b>1.3.3</b> | RPM Signals                  | 8  |
| <b>1.3.4</b> | Generating an Interrupt      | 9  |
| <b>1.3.5</b> | Versioning Data              | 9  |
| <b>1.4</b>   | VXIbus Interface             | 9  |
| <b>1.4.1</b> | Backplane Connections J1/J2  | 9  |
| <b>1.4.2</b> | Local Bus                    | 9  |
| <b>1.4.3</b> | TTL Trigger Lines            | 10 |
| <b>1.5</b>   | LEDs                         | 11 |
| <b>1.6</b>   | Installing I/O Modules       | 12 |
| <b>1.7</b>   | Technical Data               | 17 |
| <b>2</b>     | PB4350DAC1 D/A Module        | 21 |
| <b>2.1</b>   | Features and Applications    | 21 |
| <b>2.2</b>   | Block Diagram                | 21 |

|              |                                  |    |
|--------------|----------------------------------|----|
| <b>2.3</b>   | Hardware Features . . . . .      | 22 |
| <b>2.3.1</b> | Voltage Output . . . . .         | 22 |
| <b>2.3.2</b> | Reference Voltage . . . . .      | 22 |
| <b>2.3.3</b> | Floating Ground . . . . .        | 23 |
| <b>2.4</b>   | Configuration . . . . .          | 23 |
| <b>2.5</b>   | LEDs . . . . .                   | 23 |
| <b>2.6</b>   | Pin Assignment . . . . .         | 24 |
| <b>2.7</b>   | Technical Data . . . . .         | 26 |
| <b>3</b>     | Glossary . . . . .               | 29 |
| <b>4</b>     | ETAS Contact Addresses . . . . . | 31 |
|              | Index . . . . .                  | 33 |

# 1 **ES4350.1 Carrier Board**

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This section contains information about the basic features and applications of the ES4350.1 Carrier Board. A block diagram is also included here to show the schematic layout of the board.

## **note**

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*Some components of the board may be damaged or destroyed by electrostatic discharges. Please keep the board in its storage package until it is installed.*

*The board should only be taken from its package, configured and installed at a working place that is protected against static discharge.*

## **note**

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*The components, connectors and conductors of the board may carry dangerous voltages.*

*These voltages may even exist when the board is not installed in the VXI system or the VXI system is powered off.*

*Make sure that the board is protected against contact during operation.*

*Disconnect all connections to the ES4350.1 Carrier Board before removing the board from the VXI system.*

## 1.1 Features

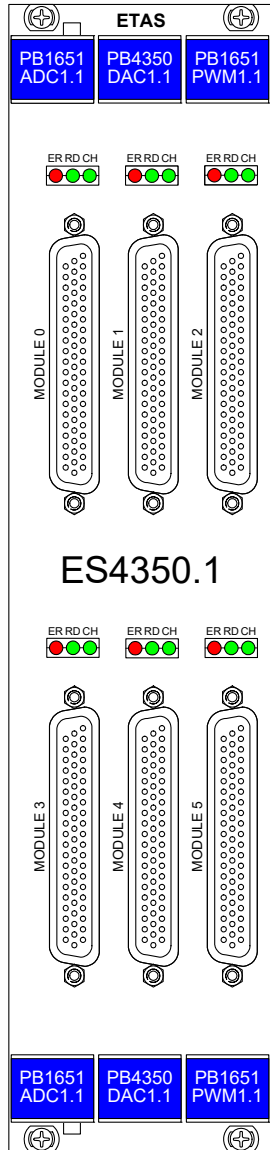
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The ES4350.1 Carrier Board acts as a carrier board for up to six I/O modules. All modules of types "PB4350XXX" and "PB1651XXX" can be used in any combination.

There are synchronization signals available for all signals generated or measured by the I/O modules of an ES4350.1 Carrier Board.

The ES4350.1 Carrier Board has a VXIbus slave interface and can generate interrupts on the backplane of the ES4300 Chassis.

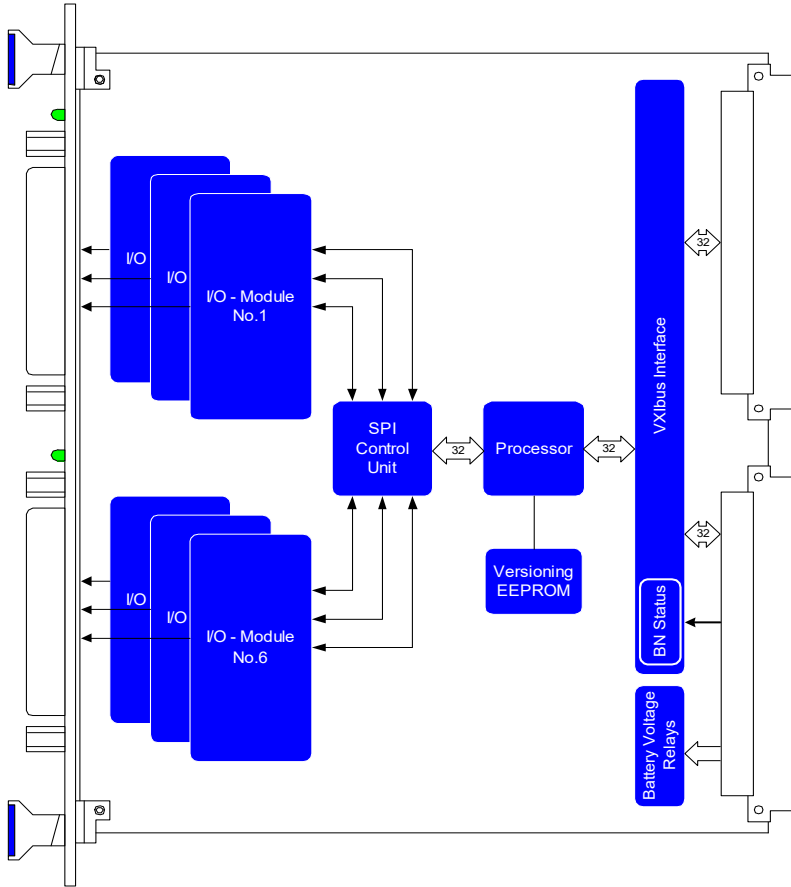
Fig. 1-1 shows the front panel of the ES4350.1 Carrier Board assembled with its maximum of six I/O modules.



**Fig. 1-1** Front Panel of the ES4350.1 Carrier Board

## 1.2 Block Diagram

Fig. 1-2 shows a block diagram with all important functional units of the ES4350.1 Carrier Board.



**Fig. 1-2** Block Diagram of the ES4350.1 Carrier Board

## 1.3 Hardware Features

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This section contains a description of the different hardware features of the ES4350.1 Carrier Board.

These are:

- "Carrier Board for Piggybacks" on page 8
- "Synchronization Signals" on page 8
- "RPM Signals" on page 8
- "Generating an Interrupt" on page 9
- "Versioning Data" on page 9

### 1.3.1 Carrier Board for Piggybacks

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The ES4350.1 Carrier Board is used as a carrier board for I/O modules in VXIbus systems. I/O modules are available for various tasks, such as the generation and measuring of ECU signals in real time.

All modules of types "PB4350XXX" and "PB1651XXX" can be used. This means that the LabCar test system can be equipped both with the standard I/O modules for the ES1651 Carrier Board (VME system) as well as with the highly precise I/O modules for the ES4350.1 Carrier Board. Up to six I/O modules of both types mentioned above can be used per ES4350.1 Carrier Board.

### 1.3.2 Synchronization Signals

---

The ES4350.1 Carrier Board also offers functions for synchronous signal generation and measuring on all I/O modules of a carrier board.

There are six synchronization signals available on an ES4350 Carrier Board. Each of these six signals is routed to each of the I/O modules – there is also a connection to the ES4350 I/O-FPGA and the VXIbus interface.

A synchronization signal can be generated from each of the described sources. A synchronization signal can be activated in the FPGA via the user interface of the ES4350.1 in the Real-Time Execution Connector.

This kind of signal can also be generated in an I/O module which is capable of generating synchronization signals via the user interface of an I/O module in the Real-Time Execution Connector.

Up to 2 synchronization signals can be transferred via the VXIbus for synchronization of several ES4350.1 Carrier Boards in one ES4300 system.

### 1.3.3 RPM Signals

---

An RPM signal is used to transfer the engine speed and consists of three individual signals, i.e. "clock cycle", "trigger" and "direction".



There are two of these RPM signals available on the ES4350.1 Carrier Board; these are routed to each I/O module. Each of the six I/O modules or one of the two RPM signals of the ES4300 Backplane can be configured as the source for an RPM signal.

Normally, an RPM signal is generated by an ES4320 VXI Signal Generator Board, output on a VXI-RPM channel to the VXIbus and routed from there to the ES4350.1 Carrier Board as an input signal on one of the two RPM signals.

### 1.3.4 Generating an Interrupt

---

With the ES4350.1 Carrier Board it is possible to generate interrupts on the backplane of the ES4300 Chassis. These can come from both an I/O module and from the processor of the ES4350.1. This means that simulation tasks can be activated on the real-time simulation processor (e.g. software tasks on the ES1130.1).

### 1.3.5 Versioning Data

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A range of versioning data is made available on the ES4350.1 Carrier Board. The board revision and PLD versions are stored in addition to the serial number; these can be read out using LabCar Operator software.

## 1.4 VXIbus Interface

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This section contains information on the assignment of the backplane connections and on how to use the "local bus" and TTL trigger lines.

### 1.4.1 Backplane Connections J1/J2

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The assignment of the backplane connections J1 and J2 adheres to the VXIbus specification. For a description, please refer to the ES4300.1 VME64x/VXI Signal Box User's Guide.

### 1.4.2 Local Bus

---

The special use of the "local bus" lines is illustrated in the table below.

| Line    | Signal (In) | J2-Pin - Row ** | Line     | Signal (Out) | J2-Pin - Row ** |
|---------|-------------|-----------------|----------|--------------|-----------------|
| LBUSA00 | +UBatt_A    | 5 - a           | LBUSC00* | +UBatt_A     | 5 - c           |
| LBUSA01 | +UBatt_A    | 6 - a           | LBUSC01* | +UBatt_A     | 6 - c           |
| LBUSA02 | +UBatt_B    | 8 - a           | LBUSC02* | +UBatt_B     | 8 - c           |
| LBUSA03 | +UBatt_B    | 9 - a           | LBUSC03* | +UBatt_B     | 9 - c           |
| LBUSA04 | -UBatt      | 11 - a          | LBUSC04* | -UBatt       | 11 - c          |

**Tab. 1-1** Using the "Local Bus" Lines

| Line    | Signal (In)   | J2-Pin - Row ** | Line     | Signal (Out)  | J2-Pin - Row ** |
|---------|---------------|-----------------|----------|---------------|-----------------|
| LBUSA05 | -UBatt        | 12 - a          | LBUSC05* | -UBatt        | 12 - c          |
| LBUSA06 | -UBatt        | 14 - a          | LBUSC06* | -UBatt        | 14 - c          |
| LBUSA07 | -UBatt        | 15 - a          | LBUSC07* | -UBatt        | 15 - c          |
| LBUSA08 | n.c./reserved | 17 - a          | LBUSC08  | n.c./reserved | 17 - c          |
| LBUSA09 | n.c./reserved | 18 - a          | LBUSC09  | n.c./reserved | 18 - c          |
| LBUSA10 | n.c.          | 20 - a          | LBUSC10  | n.c.          | 20 - c          |
| LBUSA11 | n.c.          | 21 - a          | LBUSC11  | n.c.          | 21 - c          |

\* The output lines LBUSC00 to LBUSC07 can only be carried by the signal generation board (e.g. ES4320.1) if the board in the next slot is capable of withstanding the corresponding voltages.

\*\* Non-Slot0 configuration

**Tab. 1-1** Using the "Local Bus" Lines

After powering on, the local bus connections of row a (In) and row c (Out) are not connected. The connections are only active once the ES4350.1 has been activated.

### 1.4.3 TTL Trigger Lines

The TTL trigger lines are used for the internal synchronization of the different I/O boards within the ES4300 Chassis. The TTL trigger lines are used as follows in the ES4300.

| TTL Line   | Signal              |
|------------|---------------------|
| /TTLTRG[0] | VXI_RPM_0 (Clock)   |
| /TTLTRG[1] | VXI_RPM_0 (Trigger) |
| /TTLTRG[2] | VXI_RPM_0 (UpDn)    |
| /TTLTRG[3] | VXI_SYNC_0          |
| /TTLTRG[4] | VXI_RPM_1 (Clock)   |
| /TTLTRG[5] | VXI_RPM_1 (Trigger) |
| /TTLTRG[6] | VXI_RPM_1 (UpDn)    |
| /TTLTRG[7] | VXI_SYNC_1          |

**Tab. 1-2** Using the TTL Trigger Lines

## 1.5 LEDs

The front panel of the ES4350.1 Carrier Board only has space for 3 LEDs, which are available on each of the I/O modules.

If the function of the relevant LED is independent of the special I/O module, it is described in the following table.

| LED | Color | Meaning                           |
|-----|-------|-----------------------------------|
| ER  | Red   | Error                             |
| RD  | Green | Ready                             |
| CH  | Green | The meaning depends on the module |

**Tab. 1-3** Significance of the LEDs

### *Display of the Version Number of the I/O Modules*

When the ES4300 Chassis is powered on, the I/O modules show the version number via the "RD" and "CH" LEDs. It consists of three parts (e.g. 2.1.3). First of all, the "RD" LED flashes twice ("CH" LED off). Then the "RD" LED flashes once ("CH" LED lights up). Then the "RD" LED flashes three times ("CH" LED off).

After the version number of the relevant I/O module has been displayed, the two LEDs, "RD" and "CH", go out and take on the relevant function of the I/O module used.

## 1.6 Installing I/O Modules

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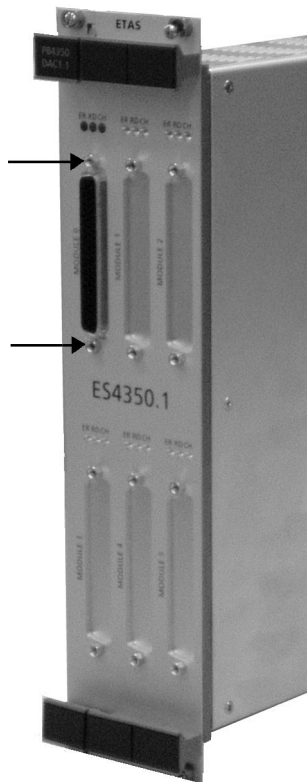
This section describes how to install another I/O module.

### *Removing the Front Panel*

---

To remove the front panel, proceed as follows:

1. Remove the screws shown in Fig. 1-3 with every I/O module already installed with a 4.5 mm socket driver.



**Fig. 1-3** Removing the Screws of Existing I/O Modules

- Slide the right-hand and middle cover out to the right (at both the top and bottom) using the handles (see Fig. 1-4).

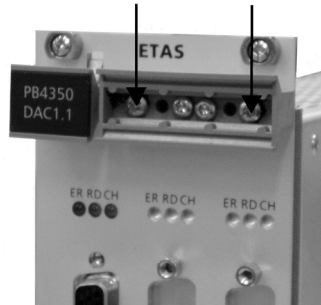
**note**

*If one or more of the four slots already contains an I/O module, remember the position of the cover to be removed!*



**Fig. 1-4** Removing the Middle and Right-Hand Handle Covers

3. Remove the left-hand and right-hand cross-recessed screw (at the top and bottom) (see Fig. 1-5). The two Torx screws in the middle must not be removed.



**Fig. 1-5** Removing the Fastening Screws from the Front Panel

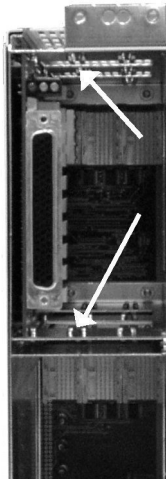
The front panel can then be removed.

#### *Installing an I/O Module*

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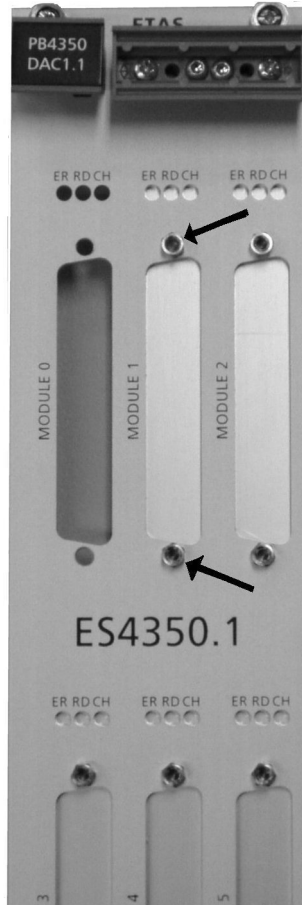
To install the new I/O module, proceed as follows:

4. Place the I/O module in the guide slots and push it to the back.



**Fig. 1-6** Guide Slots for the I/O Module

5. Remove the cover of the relevant slot attached to the front panel.



**Fig. 1-7** Screws for Fastening the Cover

### *Fastening the Front Panel*

---

To fasten the front panel back on again, proceed as follows:

6. Place the front panel on the housing of the ES4350.1 Carrier Board so that the connecting plugs of the I/O modules installed are positioned in the correct spaces of the front panel.

7. Tighten the screws loosened in step 3.  
on page 14.
8. Attach the labels removed in step 2.  
on page 13 and the new one for the I/O module installed by positioning them correctly and pushing them in.
9. Tighten the screws removed in step 1.  
on page 12 above and below the connectors available to date and the newly installed I/O module.

This completes installation.



## 1.7

### Technical Data

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This chapter contains the technical data of the ES4350.1 Carrier Board.

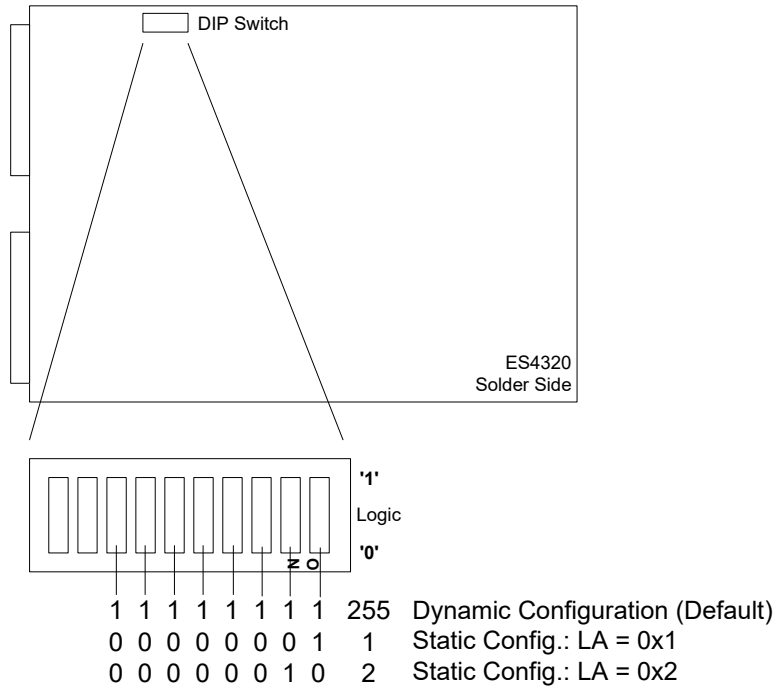
|                                    |   |
|------------------------------------|---|
| Number of slots                    | 6   |
| Supported types of I/O modules     | PB1651XXX and PB4350XXX                                   |
| Configuration of the I/O modules   | PB1651XXX and PB4350XXX, mixed                            |
| Synchronization of I/O modules     | Yes   |
| Number of synchronization signals  | 6   |
| Sources of synchronization signals | I/O module<br>ES4350.1 Processor/FPGA<br>ES4300 Backplane |

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## VXI Conformity

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|                               |  |
|-------------------------------|--|
| VXI specification             | Revision C.1, 1998   |
| Type                          | Slave  |
| Data bus                      | A16:D16<br>A24:D32, A24:D32 BLT, A24:D16   |
| Address modifier              | 2D (HEX): A16 supervisory access<br>29 (HEX): A16 non-privileged access<br>39 (HEX): A24 non-privileged data access<br>3A (HEX): A24 non-privileged program access<br>3B (HEX): A24 non-privileged block transfer (BLT)<br>3D (HEX): A24 supervisory data access<br>3E (HEX): A24 supervisory program access<br>3F (HEX): A24 supervisory block transfer (BLT) |
| Logical address<br>(see XREF) | 1-254: static assignment, DIP switch<br>0, 255: dynamic assignment, VXI resource manager   |
| Memory map                    | A16: 64 bytes<br>A24: 128 KByte  |
| Local bus lines               | Static assignments:<br>LBus[0..1] : +UBatt_A<br>LBus[2..3] : +UBatt_B<br>LBus[4..7] : -UBatt   |
| TTL trigger lines             | /TTLTRG[0..2]: VXI_RPM_0<br>/TTLTRG[3]: VXI_SYNC_0<br>/TTLTRG[4..6]: VXI_RPM_1<br>/TTLTRG[7]: VXSI_SYNC_1  |



**Fig. 1-8** DIP Switch for Creating the Logical Address

### Power Supply

|                     |                              |
|---------------------|------------------------------|
| Current consumption | 1 A @ +5 V DC (+5% - 2.5%)   |
|                     | 0.01 A @ +12 V DC (+5% -3%)  |
|                     | 0.01 A @ -12 V DC (+5% -3%)  |
|                     | 0.2 A @ +24 V DC (+5% -3%)   |
|                     | 0 A @ -24 V DC (+5% -3%)     |
|                     | 0.15 A @ -5.2 V DC (+3% -5%) |
|                     | 0.045 A @ -2 V DC (+5% -5%)  |

### *Environmental Conditions*

---

|                       |                                 |
|-----------------------|---------------------------------|
| Operating temperature | 0 °C to 70 °C (32 °F to 158 °F) |
| Relative humidity     | 0 to 95% (non-condensing)       |

---

### *Physical Dimensions*

---

|                     |  |
|---------------------|--|
| Housing (L x W x H) | 345 mm x 233.35 mm x 60.62 mm          |
| Front panel         | Height: 6 U<br>Width: 12 HP (60.48 mm) |

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## 2 PB4350DAC1 D/A Module

This chapter contains the description of the PB4350DAC1 D/A Module. It consists of the following sections:

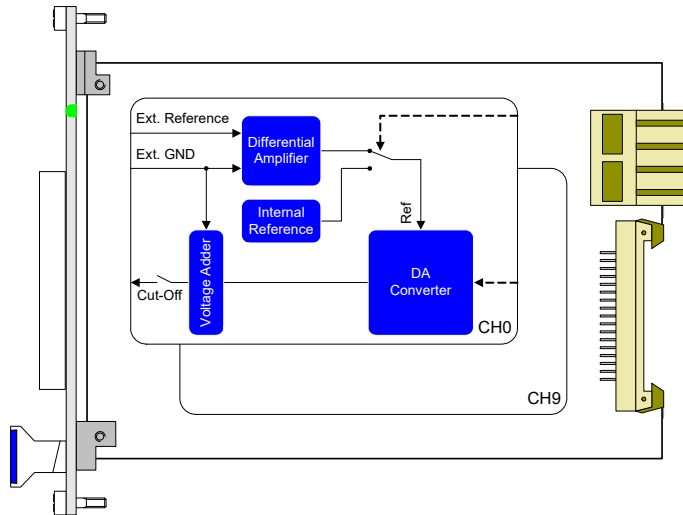
- Features and Applications (section 2.1 on page 21)
- Block Diagram (section 2.2 on page 21)
- Hardware Features (section 2.3 on page 22)
- Configuration (section 2.4 on page 23)
- LEDs (section 2.5 on page 23)
- Pin Assignment (section 2.6 on page 24)
- Technical Data (section 2.7 on page 26)

### 2.1 Features and Applications

The PB4350DAC1 D/A Module makes analog output signals with high resolution and precision available for high-end LabCars. It can be used on both VXI-bus carrier boards (ES4350.1 Carrier Board) and on VMEbus carrier boards (ES1651.1 Carrier Board).

### 2.2 Block Diagram

The following figure shows the block diagram of the PB4350DAC1 D/A Module.

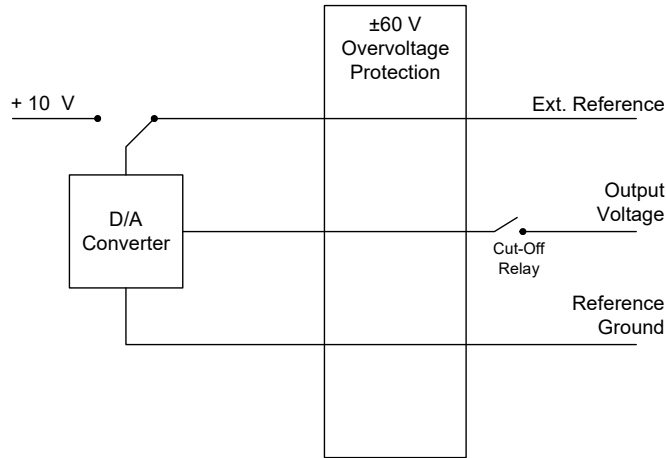


**Fig. 2-1** Block Diagram of the PB4350DAC1 D/A Module

## 2.3 Hardware Features

---

The PB4350DAC1 D/A Module has a total of ten D/A converter units which are independent of each other. The following figure shows a schematic of such a unit.



**Fig. 2-2** D/A Converter Unit of the PB4350DAC1 D/A Module

The sections below contain more details.

### 2.3.1 Voltage Output

---

The D/A converters have a resolution of 14 bits with a nominal output voltage range of 0 V to 10 V – this corresponds to a resolution of 610  $\mu\text{V}/\text{bit}$ .

The outputs of the D/A converter are routed via an output overvoltage protection which protects the module against externally applied voltages of up to  $\pm 60$  V as well as against shorts against ground.

The output signal can also be opened via a mechanical relay. This makes it possible to test an ECU connected to LabCar for its reaction to a short.

### 2.3.2 Reference Voltage

---

The user can toggle between an internal reference voltage of 10 V and an external reference specified by the user for each of the 10 D/A converter outputs of the PB4350DAC1 D/A Module. The external reference can be anywhere in the range -10 V to +10 V. ECUs typically provide a reference voltage of 5 V for analog sensors. In "Ext. reference" operating mode, the resolution can thus be doubled in the voltage range 0 ... 5 V to 305  $\mu\text{V}$ .

### 2.3.3 Floating Ground

---

For every analog signal output of the PB4350DAC1 D/A Module there is a pin on the connector for the relevant ground (Ext. GND). This makes it possible to raise or lower an output signal by a constant "offset" by specifying a specific voltage as floating ground.

**note**

*The external floating ground can be anywhere in the range -10 V to +10 V. The voltage difference between the external reference and an external floating ground can be in the range from 0 V to 10 V – this is ensured by over-voltage protection.*

**note**

*If the external ground is not used, connect this pin to AGND!*

### 2.4 Configuration

---

Signal output is configured and controlled by the Real-Time Execution Connector and LabCar Operator. A hardware configuration of the module is not necessary.

### 2.5 LEDs

---

The front panel of the ES4350.1 Carrier Board has space for the I/O connector and for 3 LEDs which every I/O module has.



**Fig. 2-3** LEDs

The LEDs of the PB4350DAC1 D/A Module have the following significance.

| LED | Color | Meaning  |
|-----|-------|--|
| ER  | Red   | Error  |
| RD  | Green | Ready  |
| CH  | Green | Flashes when displaying versioning information (see below) |

**Tab. 2-1** Significance of the LEDs

## Display of the Version Number of the I/O Modules

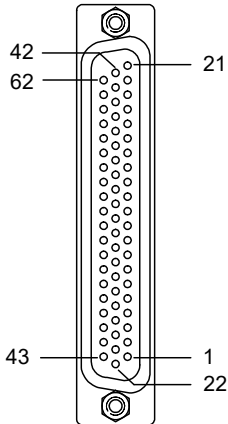
When the ES4300 Chassis is powered on, the I/O modules show the version number via the "RD" and "CH" LEDs. It consists of three parts (e.g. 2.1.3). First of all, the "RD" LED flashes twice ("CH" LED off). Then the "RD" LED flashes once ("CH" LED lights up). Then the "RD" LED flashes three times ("CH" LED off).

After the version number of the relevant I/O module has been displayed, the two LEDs, "RD" and "CH", go out and take on the relevant function of the I/O module used.

## 2.6 Pin Assignment

This section describes the pin assignment of the PB4350DAC1 D/A Module.

The connector for the signal outputs is a DSub62HD connector (female). The shielding is at front panel and housing potential and thus at protective earth.



**Fig. 2-4** Front-Facing Connector of the PB4350DAC1 D/A Module (View from the Connecting Side)



The following table contains the connector pin assignment.

| Pin | Signal  | Pin | Signal       | Pin | Signal     |
|-----|---------|-----|--------------|-----|------------|
| 1   | Out_CH0 | 22  | Ext. GND_CH0 | 43  | ExtRef_CH0 |
| 2   | Out_CH1 | 23  | Ext. GND_CH1 | 44  | ExtRef_CH1 |
| 3   | Out_CH2 | 24  | Ext. GND_CH2 | 45  | ExtRef_CH2 |
| 4   | Out_CH3 | 25  | Ext. GND_CH3 | 46  | ExtRef_CH3 |
| 5   | Out_CH4 | 26  | Ext. GND_CH4 | 47  | ExtRef_CH4 |
| 6   | Out_CH5 | 27  | Ext. GND_CH5 | 48  | ExtRef_CH5 |
| 7   | Out_CH6 | 28  | Ext. GND_CH6 | 49  | ExtRef_CH6 |
| 8   | Out_CH7 | 29  | Ext. GND_CH7 | 50  | ExtRef_CH7 |
| 9   | Out_CH8 | 30  | Ext. GND_CH8 | 51  | ExtRef_CH8 |
| 10  | Out_CH9 | 31  | Ext. GND_CH9 | 52  | ExtRef_CH9 |
| 11  | AGND    | 32  | AGND         | 53  | AGND       |
| 12  | AGND    | 33  | AGND         | 54  | AGND       |
| 13  | AGND    | 34  | AGND         | 55  | AGND       |
| 14  | AGND    | 35  | AGND         | 56  | AGND       |
| 15  | AGND    | 36  | AGND         | 57  | AGND       |
| 16  | AGND    | 37  | AGND         | 58  | AGND       |
| 17  | AGND    | 38  | AGND         | 59  | AGND       |
| 18  | AGND    | 39  | AGND         | 60  | AGND       |
| 19  | AGND    | 40  | AGND         | 61  | AGND       |
| 20  | AGND    | 41  | AGND         | 62  | AGND       |
| 21  | AGND    | 42  | AGND         |     |            |

**Tab. 2-2** Pin Assignment of the PB4350DAC1 D/A Module

## 2.7 Technical Data

This section contains the technical data of the PB4350DAC1 D/A Module in tabular form.

|   |                      |
|---|----------------------|
| Configuration   | 10 output channels   |
| Output voltage $V_{out}$  | 0 V...10 V           |
| Output overvoltage protection   | $\pm 60$ V           |
| External reference voltage  | -10 V...+10 V        |
| External GND  | -10 V...+10 V        |
| External reference to external GND  | 0 V...+10 V          |
| Analog out with ext. ref./ ratiometric  | 0...1 p.u.           |
| Output current (max.)   | 20 mA                |
| Analog output voltage resolution (internal reference)   | 610 $\mu$ V (14 bit) |
| Accuracy of analog outputs voltage $V_{out}$ in D/A converter mode with internal reference            | $\pm 5$ mV           |
| Accuracy of analog outputs voltage $V_{out}$ in D/A converter mode with external calibrated reference | $\pm 5$ mV           |
| Noise on DA outputs (10 kHz...100 MHz)  | 80 mVpp              |
| Rising time 0 V to 10 V (load of 1 k $\Omega$ in parallel with 22 pF)                                 | 50 $\mu$ s           |
| Falling time 10 V to 0 V (load of 1 k $\Omega$ in parallel with 22 pF)                                | 50 $\mu$ s           |
| Cut-off relays  | For every channel    |

### **note**

*The outputs are calibrated with a load of 1 k $\Omega$  in parallel with 22 pF.*

### **note**

*The PB4350DAC1 D/A Module can be recalibrated at ETAS. If you need a recalibration, contact your local sales office. Turn to page 31 in this manual for details of your local sales office.*

### *Power Supply*

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|                     |                    |
|---------------------|--------------------|
| Current consumption | 100 mA @ +5 V DC   |
|                     | 500 mA @ +12 V DC  |
|                     | 500 mA @ -12 V DC  |
|                     | 100 mA @ +3.3 V DC |
|                     | 100 mA @ +2.5 V DC |

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### *Environmental Conditions*

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|                       |                                 |
|-----------------------|---------------------------------|
| Operating temperature | 0 °C to 70 °C (32 °F to 158 °F) |
| Relative humidity     | 0 to 95% (non-condensing)       |

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### *Physical Dimensions*

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|                               |                 |
|-------------------------------|-----------------|
| Printed circuit board (L x W) | 145 mm x 100 mm |
| Front panel                   | Height: 3 U     |
|                               | Width: 4 HP     |

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## Glossary

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This chapter explains terms which are significant for the ES4330.1 VXI Signal Measurement Board environment.

### Battery node

Switchable battery voltage

### ES4300

The ES4300 VME64x/VXI Chassis is used to hold both new generation interface boards (VME64x, 3 U) and I/O boards which adhere to the VXI standard (ES43XX).

### ES4320

The ES4320 VXI Signal Generator Board is used to generate angle-synchronous analog signals such as, e.g., crankshaft/camshaft angle signals.

### ES4330

The ES4330 VXI Signal Measurement Board is used to acquire time- and angle-synchronous digital signals such as injection period and ignition points.

### ES1651

The ES1651 Carrier Board is used as a carrier board for PB1651XXX and PB4350XXX I/O modules. The board also has two CAN interfaces which can be configured as high speed CAN or FT-CAN.

### Real-Time I/O

The Real-Time I/O (RTIO) is the user interface of the hardware drivers which run on the I/O boards. The settings of the board can be configured here, e.g. voltage ranges, signal pre-evaluations, CAN messages etc.

### RTIO

→ Real-Time I/O

### VXIbus

VMEbus Extensions for Instrumentation. Specification based on VMEbus. The VXI specification makes several VME backplane signals available for the boards and defines the interface used to address and access these boards.



## 4 **ETAS Contact Addresses**

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### *ETAS HQ*

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70469 Stuttgart

Germany

Phone: +49 711 3423-0

Fax: +49 711 3423-2106

WWW: [www.etas.com](http://www.etas.com)

### *ETAS Subsidiaries and Technical Support*

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For details of your local sales office as well as your local technical support team and product hotlines, take a look at the ETAS website:

ETAS subsidiaries WWW: [www.etas.com/en/contact.php](http://www.etas.com/en/contact.php)

ETAS technical support WWW: [www.etas.com/en/hotlines.php](http://www.etas.com/en/hotlines.php)





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# Index

## **B**

- Backplane connections J1/J2 9
- Battery node 29
- Block diagram 7
  - ES4350.1 Carrier Board 7

## **E**

- ES4350.1 Carrier Board 5
  - block diagram 7
  - Features 5
  - technical data 17
- ETAS Contact Addresses 31

## **F**

- Front panel 6

## **G**

- Generating an interrupt 9
- Glossary 29

## **H**

- Hardware features 8

## **I**

- I/O modules
  - installing 12

## **L**

- LEDs 11, 23
- Local bus 9

## **P**

- PB4350DAC1 D/A-Module
  - block diagram 21
  - features 22
  - pin assignment 24
  - technical data 26
- Pin assignment
  - PB4350DAC1 D/A-Module 24

## **S**

- Synchronization signals 8

## **T**

Technical data

    ES4350.1 Carrier Board 17

TTL trigger lines 10

## **V**

Versioning data 9

VXIbus interface 9

    backplane connections J1/J2 9

    local bus 9